

## CMOS BCD-to-Seven-Segment Latch/Decoder/Driver For Liquid-Crystal Displays

High-Voltage Types (20-Volt Rating)

**Features:**

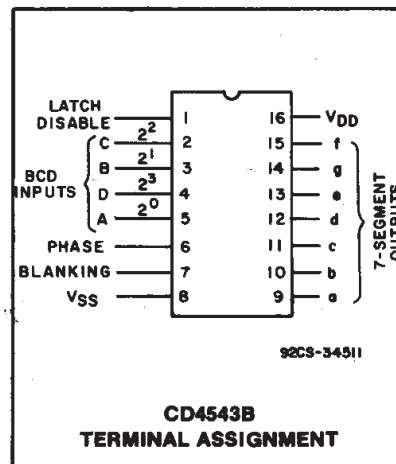
- Display blanking of all illegal input combinations
- Latch storage of code
- Capability of driving two low power TTL loads, two HTL loads, or one low power Schottky load over the full rated-temperature range
- Pin-for-pin replacement for the CD4056B (with pin 7 tied to V<sub>SS</sub>)
- Direct LED driving capability

■ CD4543B is a BCD-to-seven segment latch/decoder/driver designed primarily for liquid-crystal display (LCD) applications. It is also capable of driving light emitting diode (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement for the CD4056B when pin 7 is connected to V<sub>SS</sub>. It differs from the CD4056B in that it has a display blanking capability instead of a level-shifting function and requires only one power supply. When the CD4056B is used in the level shifting mode, two power supplies are required. When the CD4543B is used for LCD applications, a square wave must be applied to the PHASE input and the backplane of the LCD device. For LED applications a logic 1 is required at the PHASE input for common-cathode devices; a logic 0 is required for common-anode devices (see truth table).

The CD4543B is supplied in hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )	
Voltages referenced to V <sub>SS</sub> Terminal)	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V <sub>DD</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ):	
For T <sub>A</sub> = -55°C to +100°C	500mW
For T <sub>A</sub> = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C



- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V<sub>DD</sub>=5 V  
2 V at V<sub>DD</sub>=10 V  
2.5 V at V<sub>DD</sub>=15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

**Applications:**

- Instrument display driver
- Dashboard display driver
- Computer/calculator display driver
- Timing device driver (clocks, watches, timers)

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4543B Types

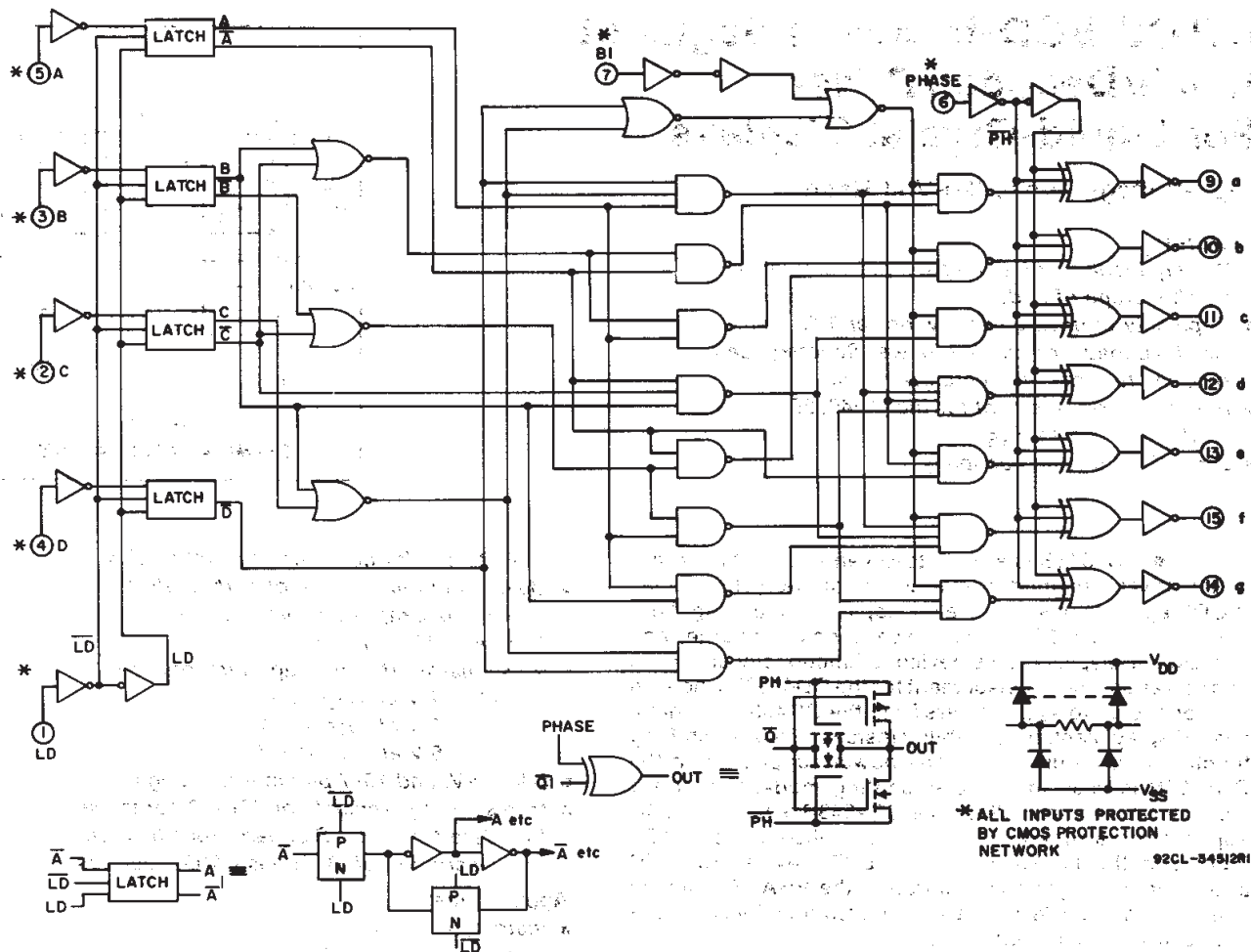


Fig. 1 - BCD-to-seven-segment latch/decoder/driver CD4543B logic circuit diagram.

## RECOMMENDED OPERATING CONDITIONS at $T_A=25^\circ\text{C}$ , Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		MIN.	TYP.	
Supply-Voltage Range (For $T_A$ =Full Package-Temperature Range)	—	3	18	V
Latch Disable Pulse Width	5	250	125	ns
	10	100	50	
	15	80	40	
Minimum Data Setup Time	5	60	15	ns
	10	20	-5	
	15	10	-5	
Minimum Data Hold Time	5	25	-5	ns
	10	20	10	
	15	20	10	

# CD4543B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current Max. I <sub>DD</sub>	—	0, 5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current Min. I <sub>OL</sub>	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min. I <sub>OH</sub>	4.6	0, 5	5	-0.46	-0.44	-0.30	-0.26	-0.37	-0.75	—	mA
	2.5	0, 5	5	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	9.5	0,10	10	-0.98	-0.92	-0.68	-0.55	-0.8	-1.6	—	
	13.5	0,15	15	-3.33	-3.18	-2.2	-1.9	-2.7	-5.4	—	
Output Voltage: Low-Level Max. V <sub>OL</sub>	—	0, 5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min. V <sub>OH</sub>	—	0, 5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage Max. V <sub>IL</sub>	0.5,4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage Min. V <sub>IH</sub>	0.5,4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current Max. I <sub>IN</sub>	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

**3**  
COMMERCIAL CMOS HIGH VOLTAGE ICs

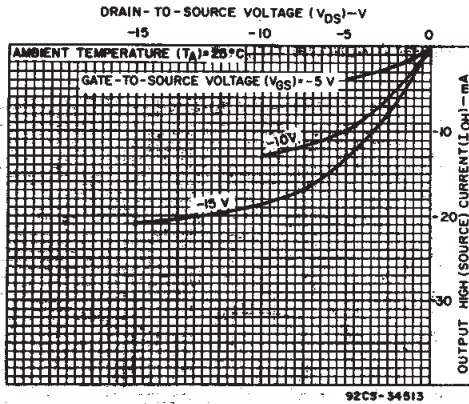


Fig. 2 - Typical output high (source) current characteristics.

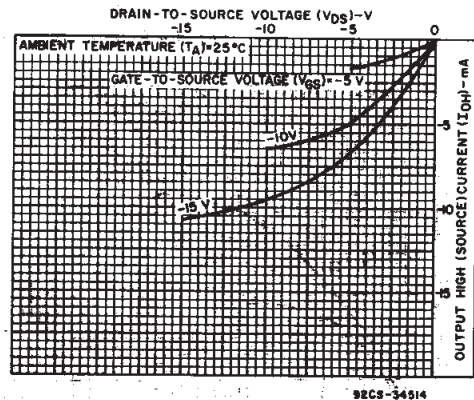


Fig. 3 - Minimum output high (source) current characteristics.

## CD4543B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A=25^\circ\text{C}$ ;  $C_L=50\text{ pF}$ , Input  $t_r, t_f=20\text{ ns}$ ,  $R_L=200\text{ k}\Omega$**

CHARACTERISTIC	TEST CONDITIONS $V_{DD}$ (V)	LIMITS All Packages			UNITS	
		MIN.	TYP.	MAX.		
Propagation Delay Time	$t_{PHL}$	5	—	600	1200	
		10	—	200	400	
		15	—	150	300	
	$t_{PLH}$	5	—	500	1000	
		10	—	200	400	
		15	—	150	300	
Transition Time	$t_{THL}$	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
	$t_{TLH}$	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
Latch Disable Pulse Width	$t_{WH}$	5	250	125	—	
		10	100	50	—	
		15	80	40	—	
Address Setup Time	$t_{SU}$	5	60	15	—	
		10	20	-5	—	
		15	10	-5	—	
Address Hold Time	$t_H$	5	25	-5	—	
		10	20	10	—	
		15	20	10	—	
Input Capacitance	$C_{iN}$	Any Input	—	5	7.5	pF

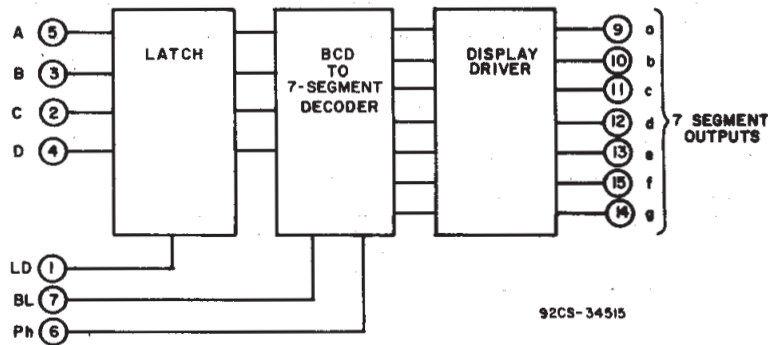


Fig. 4 - BCD-to-seven-segment latch/decoder/driver functional diagram.

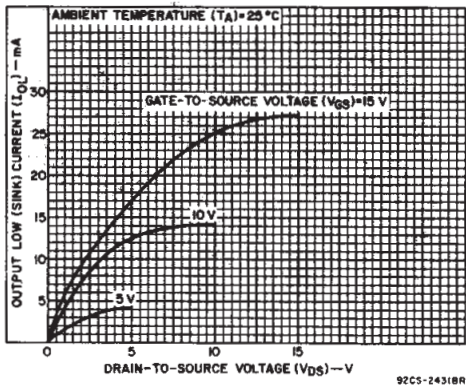


Fig. 5 - Typical output low (sink) current characteristics.

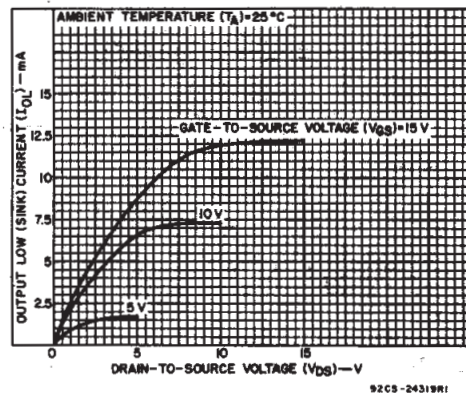


Fig. 6 - Minimum output low (sink) current characteristics.

# CD4543B Types

## TRUTH TABLE FOR CD4543B

INPUT CODE							OUTPUT STATE							DISPLAY CHARACTER
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	
X	1	0	X	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	0
1	0	0	0	0	1	0	1	1	0	1	1	0	1	1
1	0	0	0	0	1	1	1	1	1	1	0	0	1	1
1	0	0	0	1	0	0	0	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1	0	1	1	0	1	1	1
1	0	0	0	1	1	1	1	1	1	0	0	0	0	0
1	0	0	1	0	0	0	1	1	1	1	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1	1
1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
1	0	0	1	0	1	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as above

X=Don't care.

†=Above combinations.

\*=For liquid-crystal readouts, apply a square wave to Ph.

For common cathode LED readouts, select Ph=0.

For common anode LED readouts, select Ph=1.

\*\*=Depends upon the BCD code previously applied when LD=1.

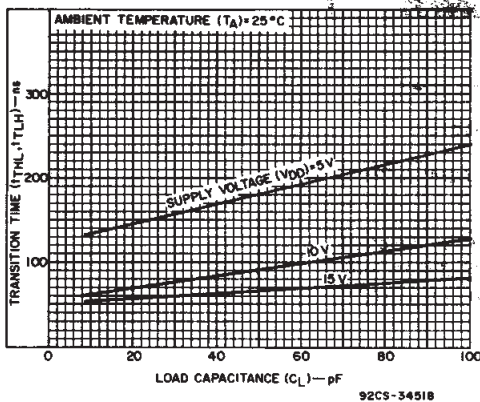


Fig. 7 - Typical transition time as a function of load capacitance.

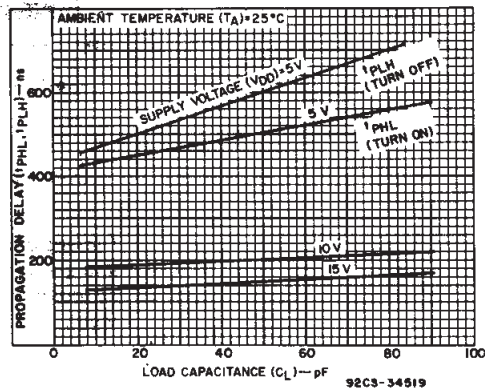


Fig. 8 - Typical propagation delay time as a function of load capacitance.

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4543B Types

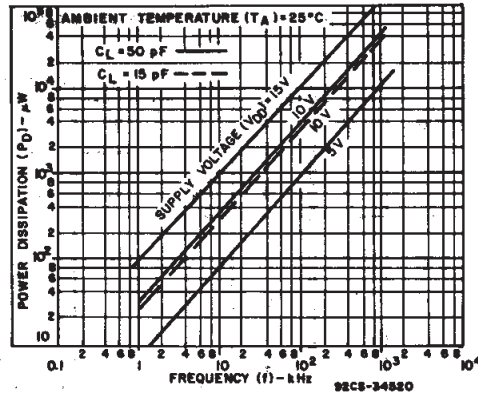


Fig. 9 - Typical dynamic power dissipation as a function of frequency.

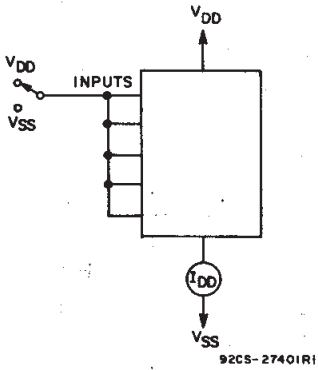


Fig. 10 - Quiescent device current test circuit.

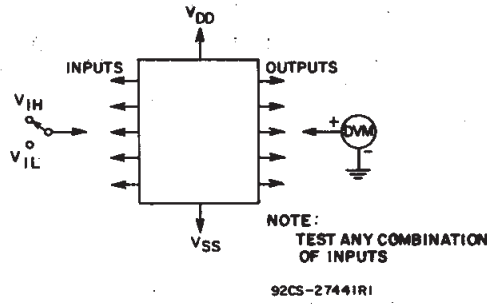


Fig. 11 - Input voltage test circuit.

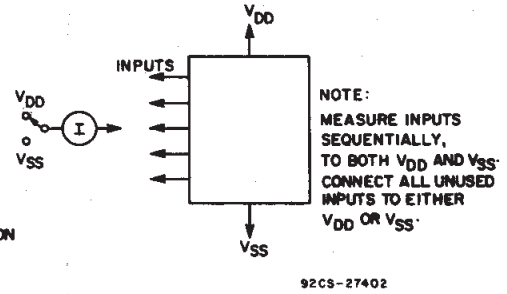
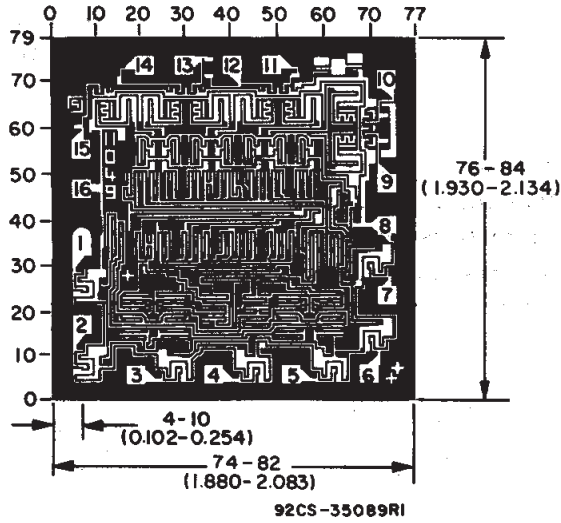


Fig. 12 - Input current test circuit.



Dimensions and pad layout for CD4543BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

This datasheet has been downloaded from:

[www.DatasheetCatalog.com](http://www.DatasheetCatalog.com)

Datasheets for electronic components.